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MOS FIELD-EFFECT-TRANSISTOR TECHNOLOGY

by W. Bösenberg and E. C. Ross

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RADIO CORPORATION OF AMERICA
RCA LABORATORIES
PRINCETON, NEW JERSEY
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SUMMARY

A two-step metallization process using aluminum for the MOS (Metal Oxide Semiconductor) transistor gate electrodes and chrome-silver for the source and drain electrodes has been developed. Silicon dioxide covers the gate electrode and insulates it from the source and drain electrodes. Work was started to encapsulate the whole integrated MOS word drive switch with a layer of phosphor silicate glass.

The oxide preparation for MOS devices was generally improved by rigorous cleaning procedures. Furthermore, a 400°C hydrogen bake decreases the surface state density at the silicon-silicon dioxide interface and makes the oxide characteristics more uniform. [100]-oriented silicon wafers show a smaller surface state density and a smaller offset voltage than [111]-oriented silicon wafers.

INTRODUCTION

The purpose of this contract is to develop the fabrication technology of silicon Metal-Oxide-Semiconductor (MOS) transistors for operating laminated ferrite memories. The ferrite memory planes require electronics along the perimeter on 0.010 in. to 0.020 in. centers. Special integrated semiconductor devices on the exact center-to-center spacing are needed. Because of the required bidirectional read-write currents, a single MOS transistor instead of a pair of npn and pnp transistors per word or digit is a simpler approach. Extremely high processing yields must be achieved in the large-scale integration that is being undertaken.

GATE METALLIZATION AND INSULATION

Previous work indicated that the use of chrome-silver metallization for the gate electrode leads to an increased number of gate shorts during life-testing. Chromium reacts with the silicon dioxide resulting in a desirable tenacious bond for the gate contacts. It is also believed, however, that this reaction is responsible for the increase in gate short circuits.

Aluminum contacts, the workhorse of integrated silicon devices, adhere well to silicon dioxide without having the gate breakdown problem. However, the formation of a thin (insulating) aluminum oxide layer makes the interconnection by means of evaporation and soldering techniques impossible. Thermocompression bonding with its pressure-temperature cycle changes the electrical characteristics of the MOS transistors and should be avoided.

A two-step metallization process was adopted. Aluminum is being used as the gate metallization. It is evaporated onto the silicon dioxide immediately after its formation to avoid contamination from the ambient. The gate contacts are then defined with photoresist and the excess aluminum is etched off. After the removal of the photoresist, a layer of a low-temperature silicon dioxide is pyrolytically deposited on top of the aluminum and on the exposed original silicon dioxide. Source and drain openings are photoetched. Chrome-silver is then evaporated over the whole surface and defined by photoetching. Thus, a structure as shown in Fig. 1 is fabricated which is similar to structures used in the fabrication of evaporated CdS thin-film transistors.

At present, the pyrolytic oxide deposition changes the transfer characteristics of MOS transistors toward the depletion mode. Therefore, a closed-loop gate is required for the transistor to be cut off by negative gate bias. For this purpose, the design of the MOS word drive switches has been modified slightly to that seen in Fig. 2.

The two-step metallization process has the advantages of a thin gate metallization which can be "burned-off" by electrical pulses in case a local gate short occurs during the fabrication process. Furthermore, the end portion of the gate metallization is covered with chrome-silver to provide a solderable contact.

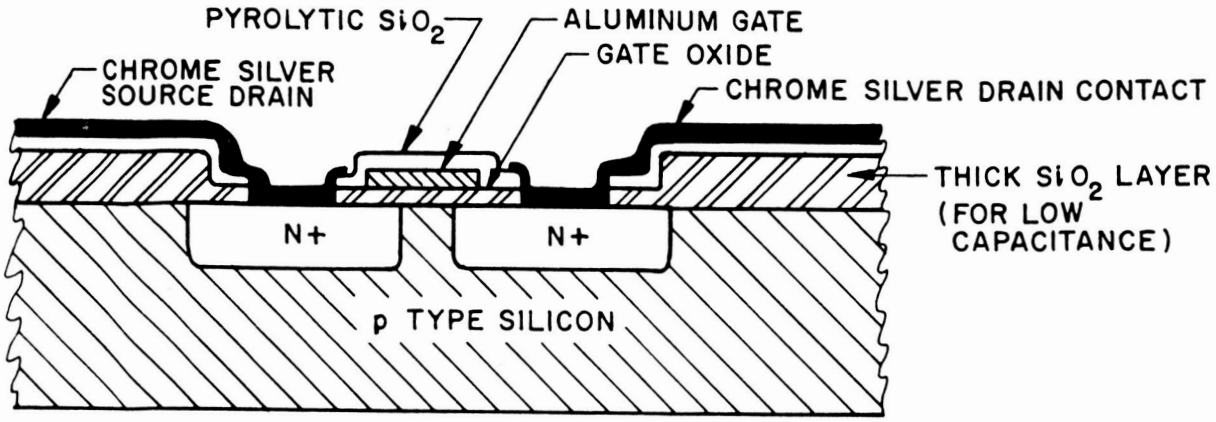

Figure 1. MOS transistor with two-step metallization.

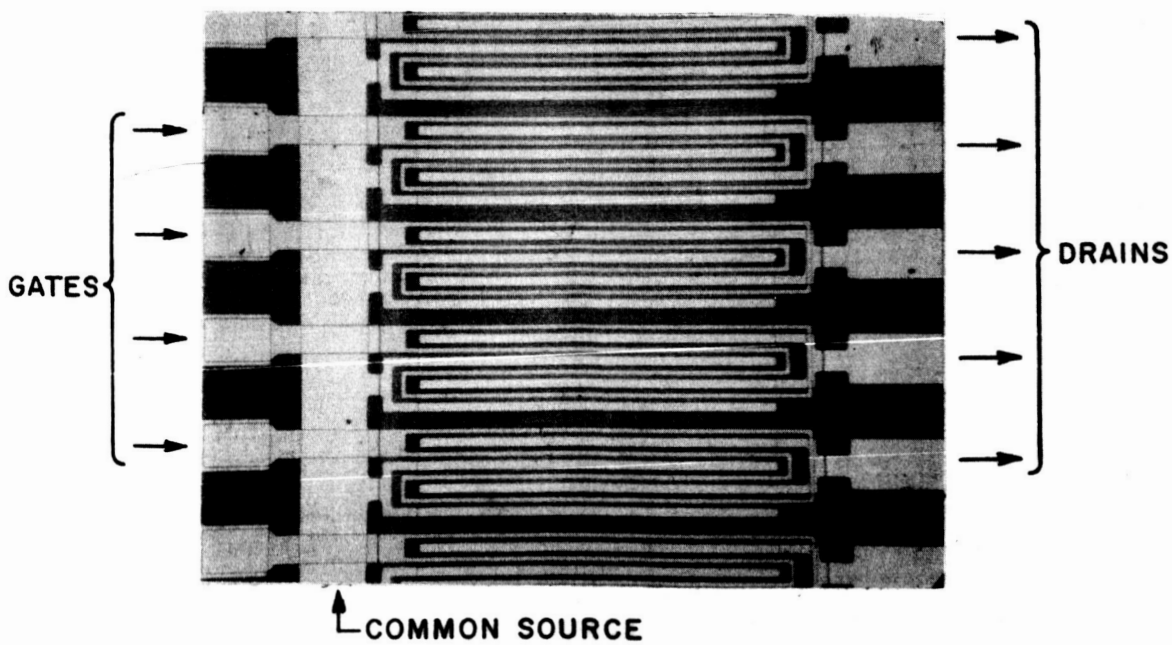

Figure 2. MOS word-drive transistor.

The gate breakdown voltage increased from an average of 15 volts to an average of 30 volts by increasing the gate oxide thickness from 300 - 400 Å to 600 - 800 Å. This decreases the transconductance of the MOS transistor, but the drain current is still sufficiently large for driving a word in the laminated ferrite memory.

The pyrolytic oxide layer also serves to insulate the source and drain leads from the gate lead at the cross-over point. This oxide layer is chemically more inert than other insulating layers previously used, including silicon monoxide and organic insulators.

HERMETIC GLASS ENCAPSULATION

A system for the low-temperature deposition of phosphor silicate glass has been set up in the laboratory. The glass is deposited through a metal mask to avoid glass deposition on the contact pads. A two-metal composition mask was used. This buckled severely due to the differential thermal expansion coefficients. A heavy molybdenum mask gives much better results, although its edge definition is not as good.

Appreciable shifts of the transfer characteristic of MOS transistors have been observed after the glass coating. The reason is not fully understood at present, and additional investigations are under way to elucidate the underlying mechanisms.

OXIDE PREPARATION

We have been able to substantially improve our channel oxides by heat-treating them in a hydrogen ambient. Figure 3 shows the superimposed MOS capacitance curves from various points of each sample surface for four different samples of channel oxide before and after hydrogen treatment. As shown in Fig. 3, before hydrogen treatment, the offset voltage (the value of the gate potential at which the capacitance is 70% of its maximum, which is approximately equal to the flat band potential) varies widely from sample to sample. Some samples even show a large spread of offset voltage measured at different points on the same sample, indicating that the oxides, as they are produced, are quite inhomogeneous.

After treatment at 400°C for 10 minutes in a partial pressure of hydrogen, the offset voltage is nearly the same for all of the samples, and the spread between offset voltages on the same sample is very small. In addition, the hydrogen bake has decreased the surface state density of the silicon-silicon dioxide interface as can be determined from the changes in the slopes of the capacitance curves. This reduction of the surface state density results in a higher value of transconductance for the MOS transistors since fewer carriers are immobilized in trapping states.

Preliminary results indicate that oxides grown side by side on silicon wafers with different crystal orientation possess different characteristics.

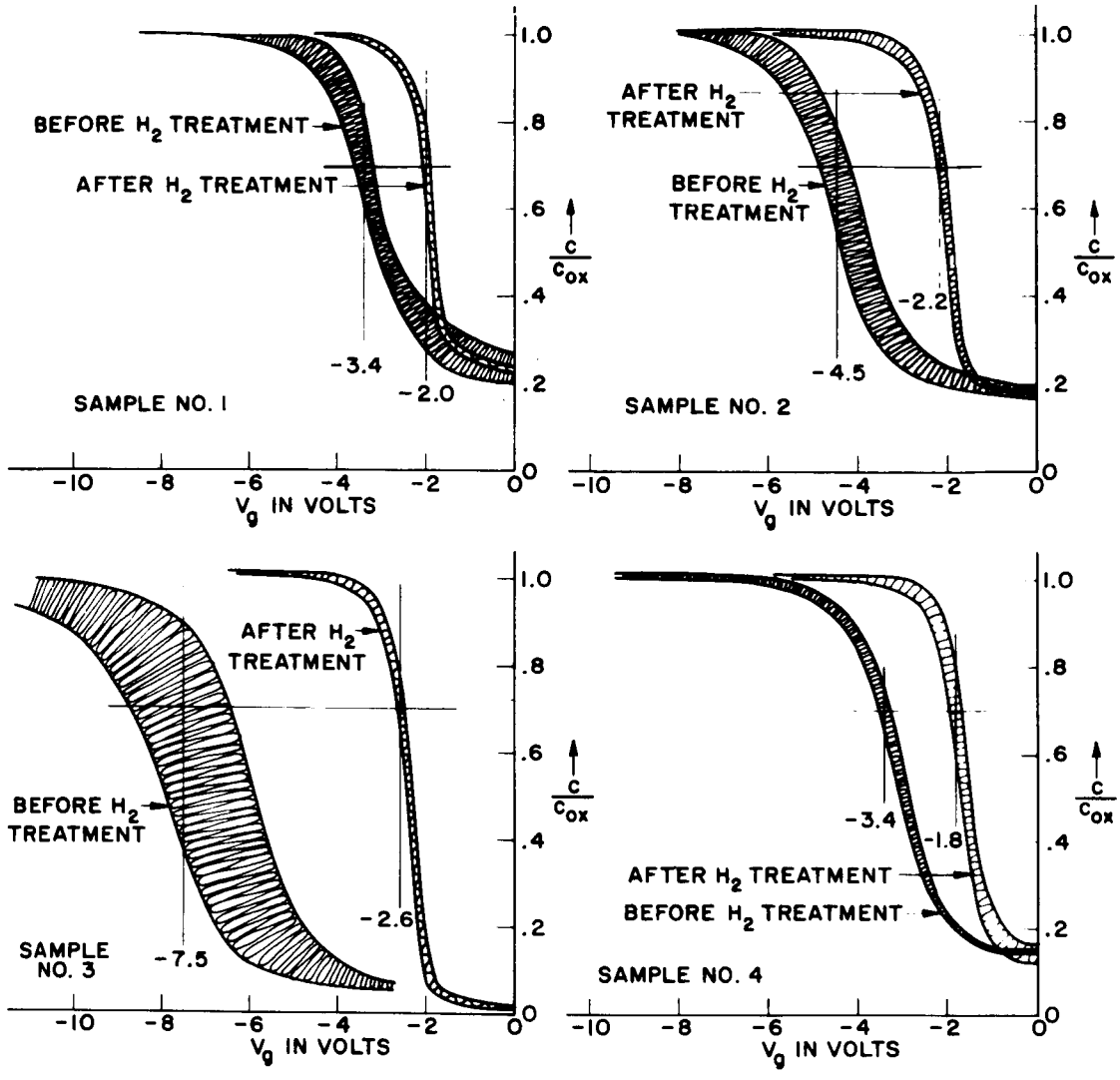

Figure 3. MOS capacitance as a function of gate voltage for four [111] silicon samples before and after hydrogen heat treatment.

Figure 4 shows the MOS capacitance curves of oxides grown simultaneously on wafers of [111]- and [100]-oriented silicon. The oxide on the [100] wafer has a smaller surface state density and a smaller offset voltage than that grown on the [111] wafer. Further work will be done in this area to determine if these results can be applied to obtain MOS transistors of superior performance compared to those fabricated on [111]-oriented silicon.

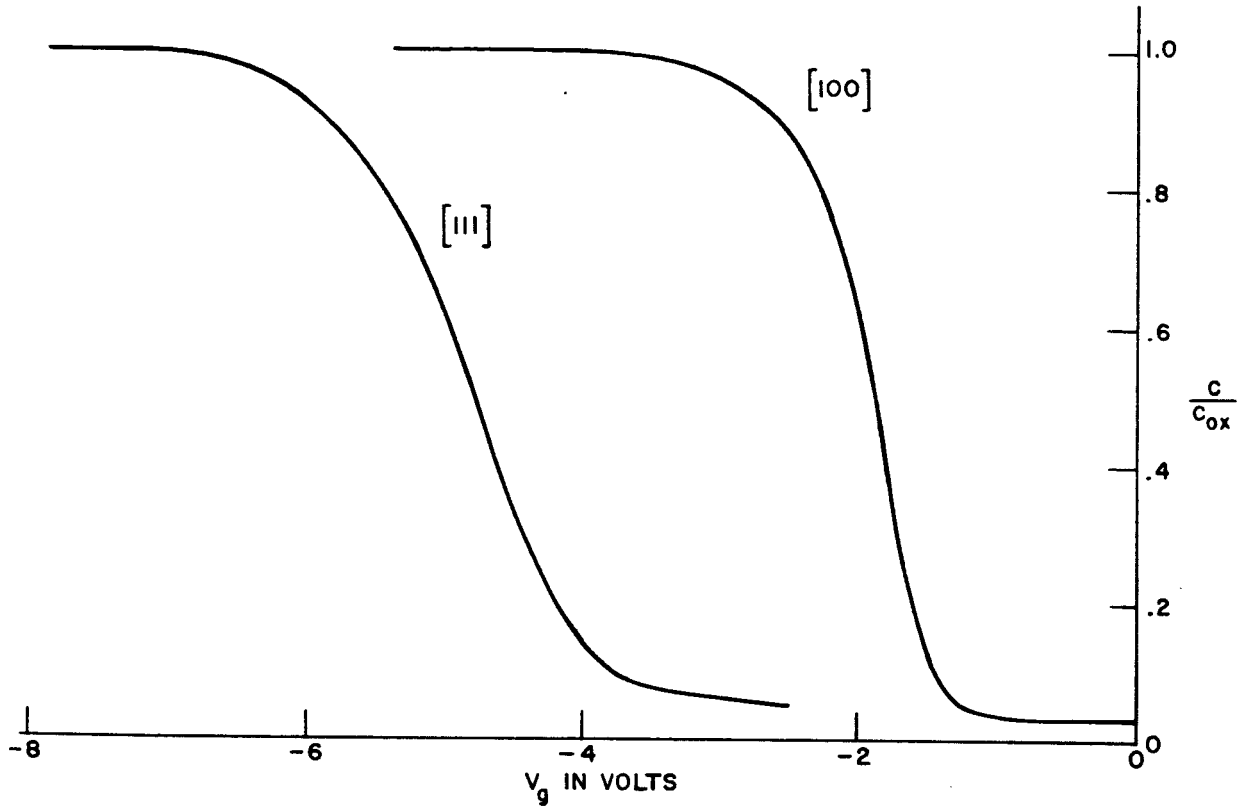

Figure 4. MOS capacitance as a function of gate voltage for a [100]- and a [111]-oriented silicon wafer of same resistivity and oxidized side by side, measured before hydrogen treatment.

CONCLUSIONS

The two-step metallization process using aluminum for the gate and chrome-silver for the source-drain electrodes has the advantages of reducing the number of gate short circuits while still maintaining solderability of the contacts. The silicon dioxide layer that is deposited at low temperatures serves as an excellent dielectric insulation between the gate and the source-drain cross-over points. It also makes the metal scratch-resistant for electrical probing of a whole wafer of integrated MOS word-drive transistors. Eventually, the whole active area will be covered with a glass layer.

The preparation of the critical channel oxide has been improved by rigorous cleaning procedures. A further hydrogen bake at 400°C reduces the surface state density and makes the electrical characteristics more uniform. Since the hydrogen baking step creates an inversion layer, the design of the MOS word-drive transistors was slightly modified to incorporate a closed-loop gate configuration. Crystal orientation is also important. [100]-oriented silicon

wafers show a smaller surface state density and a smaller offset voltage than [111]-oriented silicon wafers which were used previously.

FUTURE PLANS

The deposition of low-temperature silicon dioxide and phosphor silicate glasses will be investigated, while the electrical parameters of MOS capacitors and MOS transistors are carefully monitored. Process adjustments will be made to minimize the shift in transfer characteristics that occur during the deposition.

A semi-automatic testing system will be used to determine device yield as a function of location and to correlate it with the perfection of photo-lithographic masks.